Amendments to the Claims

1. (*Currently Amended*) A semiconductor-on-insulator (SOI) device, comprising:

at least one isolating layer made of a dielectric material;

at least one silicon substrate arranged on said isolating layer;

at least one component integrated planarly in the silicon substrate, which component has at least one slightly doped zone laterally situated between a first highly doped zone and a second highly doped zone; as well as

at least a first planar metallization region arranged between the isolating layer and the component, between the isolating layer and the slightly doped zone of the component, characterized in that at least a second planar, metallization region is arranged on the side of the silicon substrate facing away from the isolating layer, in the area of the component in the area of the slightly doped zone of the component.

2. (*Previously Presented*) A semiconductor device as claimed in claim 1, characterized in that the silicon substrate comprising the component is fixed onto the isolating layer with at least one fixing medium, with an adhesive layer.

3. (*Previously Presented*) A semiconductor device as claimed in claim 1, characterized in that

the first highly doped zone, the slightly doped zone and the second highly doped zone form at least one bipolar pnp transistor in the component; and

the slightly doped zone of the component forms the n-doped region of the pnp transistor.

4. (*Previously Presented*) A semiconductor device as claimed claim 1, characterized in that the first metallization region is embedded in at least a first oxide-based passivation layer.

5. (*Previously Presented*) A semiconductor device as claimed in claim 1, characterized in that on the side of the component facing the isolating layer, at least one oxide layer borders on at least the component or on the first passivation layer.

6. (*Previously Presented*) A semiconductor device as claimed in claim 1, characterized in that between the component and the second metallization region at least a second buried oxide-based passivation layer is arranged.

7. (*Currently Amended*) A method of manufacturing at least one semiconductor device as claimed in claim 1, wherein:

at least one isolating layer made of a dielectric material is provided with at least one silicon substrate using adhesive means;

~~at least one component having,~~ at least one component, having at least one slightly doped zone laterally situated between a first highly doped zone and a second highly doped zone, is planarly integrated in the silicon substrate; and

at least a first planar metallization region is arranged between the isolating layer and the slightly doped zone of the component, characterized in that at least a second planar metallization region is provided on the side of the silicon substrate facing away from the isolating layer, in the area of the slightly doped zone of the component.

8. (*Previously Presented*) A method as claimed in claim 7, characterized in that the first metallization region is embedded in at least a first oxide-based passivation layer.

9. (*Previously Presented*) A method as claimed in claim 7 characterized in that at least a second buried oxide-based passivation layer is arranged between the component and the second metallization region.

10. (*Currently Amended*) Application of at least a first planar metallization region as well as at least a second planar metallization region to electrically shield, on both sides, ~~at least a component~~ the at least one component incorporated in the silicon substrate of a

SOI device as claimed claim 1 to electrically shield, on both sides, ~~at least a slightly doped zone~~ the at least one slightly doped zone of the component.